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Date of Deposit: April 12, 2005

Name of Person Making Deposit: ~~Robert Faber~~ Nicole Barrese

Signature: Nicole Barrese 4/12/05

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE	
In re application of: <b>Haining Yang, et al.</b>	Date: <b>April 12, 2005</b>
Serial Number: <b>10/711,897</b>	Examiner:
Filed: <b>October 12, 2004</b>	Confirmation No: 5896
	Group Art Unit: 2811
Title: <b>METHOD AND STRUCTURE FOR IMPROVING CMOS DEVICE RELIABILITY USING COMBINATIONS OF INSULATING MATERIALS</b>	IBM Corporation D/18G, B/300, Zip 482 2070 Route 52 Hopewell Junction, NY 12533-6531

**INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Pursuant to the duty of disclosure set forth in 37 CFR 1.56, and further pursuant to 37 CFR 1.97 and 37 CFR 1.98, Applicants hereby respectfully submit copies of the non-US patents and publications as listed on Form PTO-1449, attached hereto.

Pursuant to 37 CFR 1.97 (b) (3), no fee is believed to be necessary.

Respectfully submitted,  
**Haining Yang, et al.**

By: James J. Cioffi  
James J. Cioffi, Attorney  
Registration No. 51,564  
Tel. (845)894-3363

Enclosure

FIS920040194US1

FORM PTO 1449  
(REV 2-32)U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEFile No.  
FIS920040194US1Serial No.  
10/711,897

## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use several sheets if necessary)

Applicant(s):

HAINING YANG, ET AL.

Filing Date:  
10-12-04

Group:

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	1	4,851,370	07/25/1989	Doklan et al.	437	225	12/28/1987
	2	5,506,169	04/09/1996	Guldi	437	70	10/20/1994
	3	5,538,916	07/23/1996	Kuroi et al.	437	72	04/20/1994
	4	5,580,815	12/03/1996	Hsu et al.	437	69	02/22/1994
	5	5,620,919	04/15/1997	Godinho et al.	438	230	03/30/1995
	6	5,633,552	05/27/1997	Lee et al.	310	311	07/10/1994
	7	5,668,403	09/16/1997	Kunikiyo	257	639	09/03/1996
	8	5,707,889	01/13/1998	Hsu et al.	437	69	05/13/1996
	9	5,891,798	04/06/1999	Doyle et al.	438	624	12/20/1996
	10	5,908,312	06/01/1999	Cheung et al.	438	287	05/28/1997
	11	5,985,737	11/16/1999	Wu	438	448	03/04/1998

## U.S. PATENT APPLICATION PUBLICATIONS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

## FOREIGN PATENT DOCUMENTS

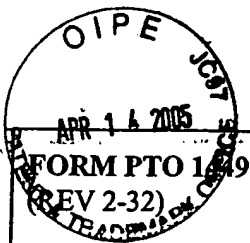
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Patents, etc.)


Examiner

Date considered

EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO 1519  
(REV 2-32)U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEFile No.  
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## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	12	5,633,202	05/27/1997	Brigham et al.	438	763	06/06/1996
	13	5,847,463	12/08/1998	Trivedi et al.	257	751	08/22/1997
	14	5,851,893	12/22/1998	Gardner et al.	438	305	07/18/1997
	15	6,040,619	03/21/2000	Wang et al.	257	649	09/25/1997
	16	6,046,494	04/04/2000	Brigham et al.	257	640	01/31/1997
	17	6,146,975	11/14/2000	Kuehne et al.	438	437	07/10/1998
	18	6,214,733 B1	04/10/2001	Sickmiller	438	691	11/17/1999
	19	6,228,777 B1	05/08/2001	Arafa et al.	438	740	06/08/1999
	20	6,261,924 B1	07/17/2001	Mandelman et al.	438	430	01/21/2000
	21	6,306,742 B1	10/23/2001	Doyle et al.	438	591	01/05/1999
	22	6,395,610 B1	05/28/2002	Roy et al.	438	354	06/20/2000

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FORM PTO 1449  
(REV 2-32)

U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE

File No.  
FIS920040194US1

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	23	6,436,848 B1	08/20/2002	Ramkumar	438	777	03/30/1999
	24	6,476,462 B2	11/05/2002	Shimizu et al.	257	627	12/07/2000
	25	6,509,230 B1	01/21/2003	Roy et al.	438	261	06/20/2000
	26	6,515,351 B2	02/04/2003	Arafa et al.	257	644	02/28/2001
	27	6,573,172 B1	06/03/2003	En et al.	438	626	09/16/2002
	28	6,724,053 B1	04/20/2004	Divakaruni et al.	257	402	02/23/2000
	29	6,825,529 B2	11/30/2004	Chidambarao et al.	257	336	12/12/2002

U.S. PATENT APPLICATION PUBLICATIONS

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**INFORMATION DISCLOSURE CITATION**  
*(Use several sheets if necessary)*

 ATTY DOCKET NO.  
 FIS920040194US1

 APPLICATION NO.  
 10/711,897

HAINING YANG, ET AL.

 FILING  
 10-12-04

GROUP ART

**U.S. PATENT DOCUMENTS**

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**U.S. PATENT APPLICATION PUBLICATIONS**

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

**FOREIGN PATENT DOCUMENTS**

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO

**OTHER DOCUMENTS** *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	1	T. H. Ning; "Why BiCMOS and SOI BiCMOS?;" IBM J. Res & Dev. Vol. 46 No. 2/3 March/May 2002; pages 181 - 186..
	2	T. G. Berence et al., "The Combined Effects of Deuterium Anneals and Deuterated Barrier-Nitride Processing on Hot-Electron Degradation in MOSFET's;" IEEE Transactions of Electron Devices, Vol. 46, No. 4, April 1999; pages 747 - 753.

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**FOREIGN PATENT DOCUMENTS**

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						YES	NO

**OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)**

J. H Stathis; "Reliability limits for the gate Insulator in CMOS technology;" IBM J. Res & Dev. Vol. 46 No. 2/3 March/May 2002; pages 265 - 286.

3

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